DC Bias Test in Soft Ferrite Cores

Presenting By:
The Team,
Speedofer Components Pvt. Ltd.

Technical Inputs:
Probal Mukherjee,
The Head, Technical
probal@speedofer.com

Pen:
Emmanuel David,
The Manager, R&D
ed@speedofer.com

Update:
Jan 2015

DC Bias Test: An Understanding

- Any PCBA (PCB Assembly) to run, certain amount of Power is designed to be given in the form of IDC (DC Current) of which the magnetic material in the Driving Transformer or an Inductor needs to withstand in the application or the field.

- In the process, the device will be evaluated by applying the maximum Current that is expected to be drawn by the PCBA during the application. Also, one can derive the I_{SAT} (Current Saturation Point) or an amount of Current that the device is able to withstand so as to ensure the Product will perform better in maximum operating Current in the application.

- As a thumb rule, I_{SAT} of any Transformer or an Inductor must be measured at anywhere after half the value of L_0 or Initial Inductance so as to ensure the device is potentially qualified on this parameter.

- As the typical specification, the Product Designer of OEM or ODM (Original Equipment Manufacturer or Original Design Manufacturer) would specify as 90% of L_0 at 25°C; 1kHz / 10kHz / 50kHz; 300mV / 1000mV at *certain* Current Level.

DC Bias Test Technical Aspects & Advantages

- DC bias measurement of E shaped Ferrite Cores in CFL / Ballast / LED Lighting is a direct measure of the I_{SAT} and loop squareness. Hence, it is a sure test to ascertain that the correct specified material has been used without any mix-up in the Powder Metal Composition.

- In case there is a mix up in Ferrite material, the AL value may be okay but the Cores would fail in actual application when the full load Current of the PCBA passes through the E Core choke. The Ferrite Cores material may *Saturate* well before the required level thus causing a failure of the Lamp which might lead to a burn-out.

- Conducting the test in a temperature oven with a thermal temperature profile in different temperature cycles can characterize or classify the temperature variation of the material. However, this is done for the critical applications as these would increase the operational costs.

- If the Ferrite Core fails to withstand at the premature stage than specified Current being given through the Circuit in the application, Circuit Frequency will go higher than specified due to an inrush Current to the Circuit. When the Frequency goes higher than specified, the Temperature / the Heat will increase. When the Temperature / Heat goes higher than specified, a part or the full Circuit Board will get burnt.

- DC Bias Test at high temperatures may show up any hidden sinter cracks in Ferrite Cores.

- DC Bias Test conducted with actual bobbin help simulate actual Circuit condition.

- AL Value matching with respect to the specification does not mean that the Ferrite will be thorough with the DC Bias Performance.

DC Bias Application Specific (Why in Lighting (CFL / Ballast / LED Industry)

- As a part of Product Reliability test, CFL / Ballast / LED Lighting assemblies are being tested at elevated environments or the test conditions in multiple time cycles. A failure of a ferrite core I_{SAT} may occur at such test conditions which leads in increasing the frequency of PCBA and thus the overall temperature & heating of PCB assembly.

- In the specific time zones for these severe conditions, CFL / Ballast / LED Lighting circuits fail and hence, it is essential to ensure an adequate I_{SAT} level of the E core.

- As the reliability test in elevated test conditions is an expensive affair, one can measure DC bias instead and empirically correlate by specifying a No Go limit.

DC Bias: A Challenge to the Ferrite Cores Eco System

- *Ferrite Core Manufacturers Challenge*: I_{SAT} of Ferrite Cores can be improved by Metal Composition of Powder. Once that is established, the Saturation of the core is controlled by the densification during the manufacturing.
  When Metal Composition of Powder including the Particle Size Distribution (PSD) is wrong, one may expect almost 100% failure in DC Bias Performance Test.

  When the densification problems during the manufacturing exists, FRACTIONAL or PARTIAL failures within the batch of material produced would occur even with the RIGHT Metal Composition of the Powder. The densification to be appropriated without any effect on dimensions and bending of which the actual tuning of the below parameters to be done by the Sintering Process expert.

  RIGHT Loading Pattern, RIGHT N_2 (Nitrogen) Thermal Profile, RIGHT Soak temperature, RIGHT Cooling time

  Maintaining the RIGHT densification would clash with the product throughput and one may have to forgo that to a bit of an extent to ensure proper I_{SAT} of the Cores.

  To make each & every device that being taken up for this test needs to be prepared as fully finished bobbin as the Transformer or an Inductor before Testing.

- *EMS (Transformer or Inductor Assemblers) Challenge*: Omitting this measurement before assembly would lead to expensive market failure for the lamp manufacturer. OEM or ODM overwrites I_{SAT} specification than actual requirement to ensure no potential failure due to this.

- *OEM & ODM Challenge*: Inconsistent operating environments in different Geographies

DC Bias Specification Calculation (Design Specific)

- DC Bias value of a particular circuit shall be derived with the pre requisite of TRUE RMS Current of actual choke in the highest input Voltage of the lamp (320V) with the below method.

- Measure actual TRUE RMS Current in the Choke (PCB Circuit) at the highest input voltage of the lamp (320V). (EMS has to get from OEM / ODM and share the values to the Ferrite Core Supplier)

- Measure the actual TRUE RMS Voltage across the choke at the highest input voltage of the lamp and also measure the lamp frequency in kHz.

- The DC Amp is the True RMS Current with the same condition in which the circuit designed to operate (Number of turns, Wire Diameter, AL Value and the tolerance), Inductance has to be remained at >90% of L_0 (Initial Inductance) when Biasing current.

$$\text{Current} = \frac{\text{RMS Voltage}}{2\pi \text{ frequency (kHz)} \times \text{L (mH)}}$$

$$\text{DC} = \text{Current} \times \frac{\sqrt{3}}{2} \text{ Amps}$$

At this level of DC in Amps, Cores must retain a minimum of 90% of the Initial Inductance.

Notes:
OEM / ODM needs to educate Transformer or Inductor Assemblers on this method for effective management.
Ferrite Core Suppliers cannot derive the TRUE RMS Current of the actual choke at the highest input voltage (320V)

DC Bias Test Sample Size

- Sample size for DC Bias Test has always been on an empirical way and however, the best sample size that one shall be adopted would be the below.

- However, Ferrite Core Supplier has to be given the Test Coils for executing this exercise as Ferrite Core Supplier does not assemble Transformer / Inductor on its own.

Material in Pieces	100000	40000	10000	4000
Sample Size	40	25	15	10
Sample Size in Percentile	0.04	0.0625	0.15	0.25

DC Bias Test Specimen Graphical Information

Speedofer Components Pvt. Ltd.

System Compliance	ISO 9001:2008 Quality Management System	Revision	0
Document Name	SCPL Saturation Current I_{SAT} / I_E Measurement	I_{SAT} / I_E Measurement	
Document No	SCPL-QMS-R&D-F-01		

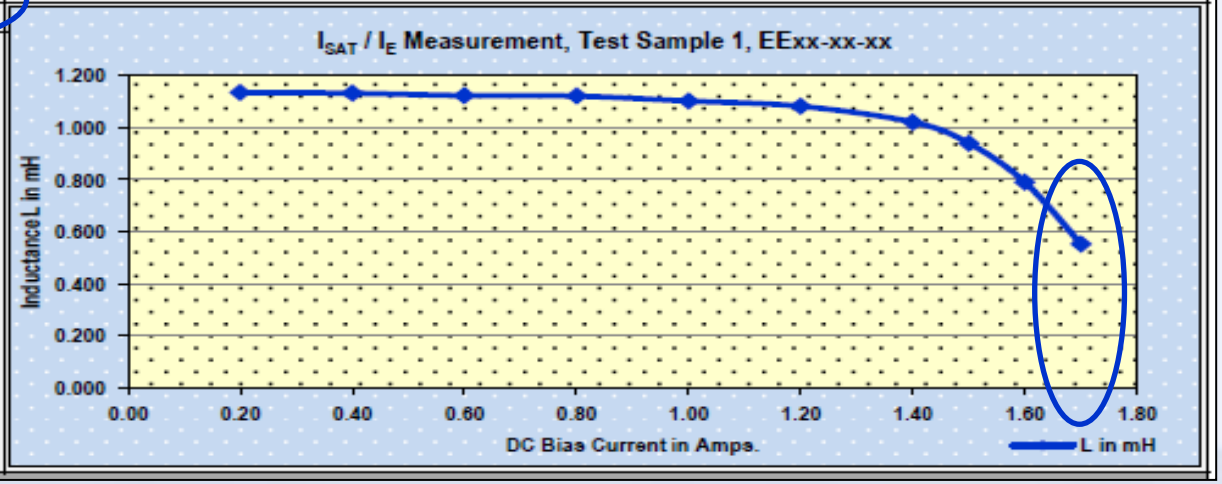
Ferrite Core Configuration Details		Test Condition Details		Test Instruments Details	
Geometry	XXX	Temperature in °C	25 ± 3°C	Dimmer	NA
AL Value Spec	xxx	Frequency in kHz	1kHz	DC Bias Meter	xxx
Inductance Spec	xxx	Voltage in mV	300mV	LCR Meter	xxx
Source	xxx	Coil Wire Diameter	NA		
Material Type	xxx	No of Strands	NA	Remarks	
Lot	xxx	No of Turns	NA		
Date	xxx	Test Coils Prepared	Client	Client:	xxx
Remarks	None	Remarks			

Parameters		Reference
*Initial Inductance L_0 in mH (Measured)		*'Initial Inductance L_0 in mH (Measured)' to be measured before DC Bias
**50% of Inductance L in mH at Saturation Point I_E (Expected)		**'50% of Inductance L in mH at Saturation Point I_E (Expected)' considered as a rule of thumb
Specified Saturation Point I_E in Amps. (Spec)	NA	***To measure 'Reduced % of Inductance L_0 in mH at Saturation Point', refer Inductance observed at Saturation & 'Initial Inductance L_0 in mH (Measured)'
Actual Saturation Point I_E in Amps. (Actual)	mH	
***Reduced % of Inductance L_0 in mH at Saturation Point I_E	50%	

Measured Values

Test Sample 01			L0	50%of L0
Step	I in Amps	L in mH	1.14	0.57
1	0.20	1.135		
2	0.40	1.132		
3	0.60	1.123		
4	0.80	1.121		
5	1.00	1.102		
6	1.20	1.082		
7	1.40	1.021		
8	1.50	0.940		
9	1.60	0.790		
10	1.70	0.553		
11				
12				
13				
14				
15				

Current Vs. Inductance Curve



DC Bias Test Specimen Graphical Information

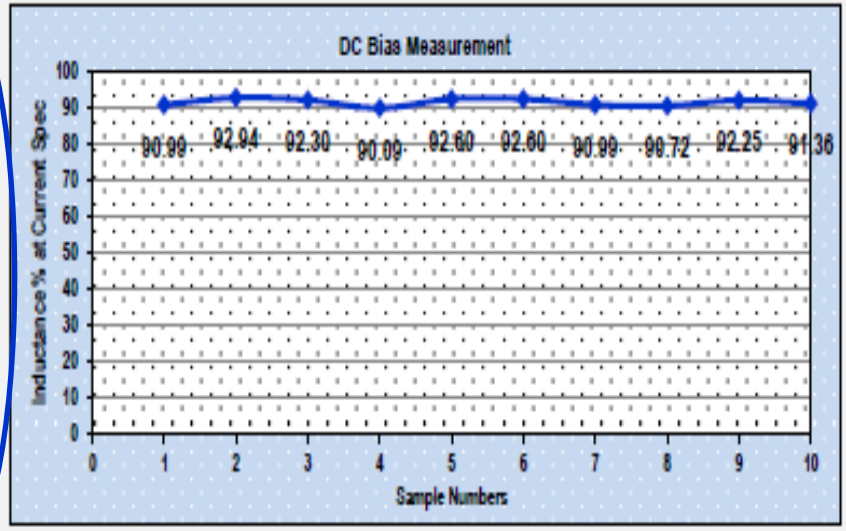
Speedofer Components Pvt. Ltd.

System Compliance	ISO 9001:2008 Quality Management System	Revision	0
Document Name	SCPL DC Bias Measurement Report	I_{SAT} / I_E (DC Bias) Measurement Report	DC Bias Test
Document No	SCPL-QMS-RD-F-02		

Geometry	xx-xx-xx	DC Bias	xxx							Date	xx-xx-xxxx
AL & Combination	xxx	Dimmer	xxx							Client Name	xxx
Core Combination	xxx	LCR	xxx							Lot Number	xxx
Inductance	xxx	Test Condition	Temp	f	V	L0	I	Wire Dia	Strands	Turns	File Revision	0
			25°C±3	1kHz	300mV	90%	1.4A	NA	NA	147		
Make	Speedofer	Client Spec	≥90% of L0 (Initial Inductance) at 1kHz, 300mV, 1.4Amps									
Material Type	xxx											

Achieved Values

Sample	L0 in mH	L in mH at 1.4A	L % at 1.4A
1	1.110	1.010	90.99
2	1.091	1.014	92.94
3	1.091	1.007	92.30
4	1.110	1.000	90.09
5	1.095	1.014	92.60
6	1.095	1.014	92.60
7	1.11	1.01	90.99
8	1.11	1.007	90.72
9	1.11	1.024	92.25
10	1.099	1.004	91.36



DC Bias Test Specimen Graphical Information

Speedofer Components Pvt. Ltd.

System Compliance	ISO 9001:2008 Quality Management System	Revision	0
Document Name	SCPL Saturation Current I_{SAT} / I_E Measurement	I_{SAT} / I_E Measurement	
Document No	SCPL-QMS-R&D-F-03		

Ferrite Core Configuration Details		Test Condition Details		Test Instruments Details	
Geometry	xxx	Temperature in °C	25 ± 5°C	Dimmer	NA
AL Value Spec	xxx	Frequency in kHz	1kHz	DC Bias Meter	xxx
Inductance Spec	xxx	Voltage in mV	300mV	LCR Meter	xxx
Source	Speedofer	Coil Wire Diameter	NA	Remarks	NA
Material Type	xxx	No of Strands	NA		
Lot	xxx	No of Turns	280		
Date	xxx	Test Coils	Client		
Combination	xxx	Remarks	NA	Client:	xxx

Parameters		Reference
*Initial Inductance L_0 in mH (Measured)	1.906mH	*'Initial Inductance L_0 in mH (Measured)' to be measured before DC Bias
**50% of Inductance L in mH at Saturation Point I_E (Expected)	0.95325mH	**'50% of Inductance L in mH at Saturation Point I_E (Expected)' considered as a rule of thumb
Specified Saturation Point I_E in Amps. (Spec)	NA	***To measure 'Reduced % of Inductance L_0 in mH at Saturation Point', refer Inductance observed at Saturation & 'Initial Inductance L_0 in mH (Measured)'
Actual Saturation Point I_E in Amps. (Actual)	1.4–1.5 Amps.	
***Reduced % of Inductance L_0 in mH at Saturation Point I_E	50%	

Measured Values

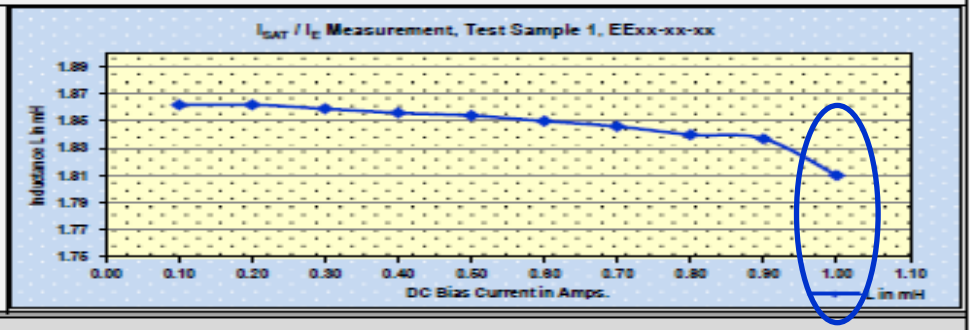
Test Sample 01

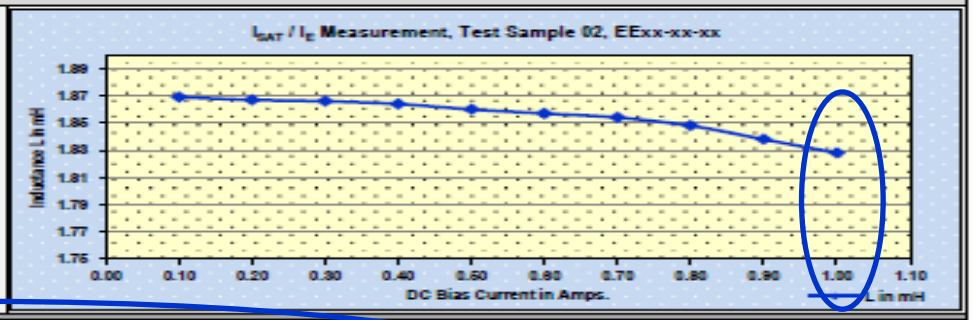
Step	I in Amps	L in mH
1	0.10	1.86
2	0.20	1.86
3	0.30	1.86
4	0.40	1.86
5	0.50	1.85
6	0.60	1.85
7	0.70	1.85
8	0.80	1.84
9	0.90	1.84
10	1.00	1.81
11		
12		
13		
14		
15		

Test Sample 02

Step	I in Amps	L in mH
1	0.10	1.87
2	0.20	1.87
3	0.30	1.87
4	0.40	1.86
5	0.50	1.86
6	0.60	1.86
7	0.70	1.85
8	0.80	1.85
9	0.90	1.84
10	1.00	1.83
11		
12		
13		
14		
15		

Current Vs. Inductance Curve





Client Specifications			Measured Values				Calculations		Remarks
L in mH	I in Amp	% of L Value	Sample No	L_0 in mH (Before DC Bias)	L mH at Specified DC Bias	I in Amp at L Specified	% of L Value	80% of L Value	
1.9	0.7	80% of L_0	1	1.906	1.848	1.4–1.6	96.903	1.715	
1.9	0.7	80% of L_0	2	1.908	1.864	1.4–1.6	97.170	1.717	

Thank You

Emmanuel David,
Manager, R&D.

Speedofer Components Pvt. Ltd.,
Plot No: 101 & 102, Toy City,
Ecotech – III, Greater Noida – 201306,
Uttar Pradesh, India.
HP: +91 991 009 4723, DID: +91 120 239 7116 - 117.
URL: http://www.speedofer.com
Recognition of In-House R&D Unit by DSIR, Government of India: No. TU/IV-RD/3837/2015
Facebook: https://www.facebook.com/speedofer